REMARKS

Claims 1-6 are all the claims pending in the application.

Statement of Substance of Interview

As an initial matter, Applicants' representative thank the Examiner for the courtesies extended during the telephonic interview conducted on April 16, 2009. In view of the helpful comments provided by the Examiner during the interview, Applicants submit herewith the arguments presented during the interview with respect to the 35 U.S.C. § 112 rejection. Further, in accordance with the Examiner's instructions, Applicants kindly request the Examiner to call the Applicants' representative at the number listed below (on page 12) to discuss the Applicants' arguments after reviewing the instant Amendment and prior to issuing any subsequent action.

It is respectfully submitted that the instant STATEMENT OF SUBSTANCE OF INTERVIEW complies with the requirements of 37 C.F.R. §§1.2 and 1.133 and MPEP §713.04.

Claim Rejections – 35 U.S.C. § 112

Claims 5 and 6 stand rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement. For *at least* the following reasons, Applicants respectfully traverse the rejection.

Applicants submit that the arguments submitted in the previous Amendment filed October 8, 2008 sufficiently pointed out portions of the Specification and drawings which support the features recited in claims 5 and 6. In response to these arguments, the Examiner confusingly, and inaccurately, asserts that the middle column of FIG. 3 ('Rise/fall') is "totally incorrect" (Office Action, page 15, last paragraph, and page 17, first paragraph). Specifically,

the Examiner thinks that the determination that no delay ('NONE') was caused by the input, as recited in claim 6, is incorrect. Applicants respectfully disagree.

For instance, as discussed in the Specification, and as pointed out during the aforementioned phone interview, since the state of the output is low both at the first clock signal (when input 1 rises), and at the second clock signal (when input 2 falls), it is determined that no delay was caused by the input (Specification, page 7, line 22 to page 8, line 6, and FIG. 3). As such, contrary to the Examiner's assertions, the determination of 'NONE" in FIG. 3 is justified.

Claim 5 recites that the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed.

At least page 7, line 22 to page 8, line 6 of the Specification, and FIGS. 3-5 of the Applicants' drawings support the above-noted features of claim 5. FIG. 3 is a waveform diagram showing the rise and fall delay patterns of a 2-input AND circuit, according to a non-limiting, exemplary embodiment of the present invention. That is, FIG. 3 is an example of the claimed delay time information in the delay analysis library. In the case where the input 1 rises and the input 2 falls, the Specification discloses that "no terminal is selected for delay analysis" (Specification, page 8, lines 5 and 6). That is, when no change in a signal state of an output terminal of the logical circuit is determined (see FIG. 3, middle column – 'Rise/fall'), the delay analyzing module determines that no further delay analysis needs to be performed. Moreover, this determination is necessarily automatic since it is based on the logical operation information

of the logical circuit, which is stored in the delay analysis library. Therefore, Applicants respectfully submit that claim 5 complies with the requirements of 35 U.S.C. § 112.

Applicants further submit that the features of claim 6 are supported by the Applicants' disclosure. For example, claim 6 recites that the logical circuit is an AND gate, and when the logical operation information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals, and at a time at which the second clock signal among the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case.

Applicants respectfully submit that the portions of the Specification and Applicants' drawings discussed above with respect to claim 5 also support the features of claim 6. It appears that the Examiner's position is that since the claim features at issue are allegedly not found explicitly in the Applicants' Specification, the subject claim limitations must not be supported by the Applicants' disclosure. **Applicants respectfully submit, however, that there is no *in haec verba*—i.e., word for word—requirement for satisfying the written description requirement.** Therefore, contrary to the Examiner's assertions, Applicants are not burdened to show where the claimed terms are explicitly recited in the Specification. **Rather, the newly added claim limitations can be supported in the Specification through express, implicit, or**

inherent disclosure (*Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997 as cited in MPEP § 2163.02). Additionally, Applicants can show possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as **words, structures, figures, diagrams, and formulas** that fully set forth the claimed invention. *Id.*

Here, in a non-limiting, exemplary embodiment of the claimed delay time information shown in FIG. 3, it is shown in the middle column of the table in FIG. 3 (the 'Rise/fall' column) that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals. Further, it is shown that at a time at which the second clock signal among the two clock signals is input, the state is LOW which is the same state as the first signal state (i.e., at the first clock signal). Accordingly, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to the clock signal (see Specification, page 8, lines 5 and 6), and thus, in this case the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate. Therefore, the delay analyzing module, based on this delay time information, automatically determines that no further delay analysis needs to be performed as recited in claim 6. *Id.* As such, Applicants respectfully submit that claim 6 complies with the requirements of 35 U.S.C. § 112.

Claim Rejections – 35 U.S.C. § 101

Claim 3 is rejected under 35 U.S.C. § 101 because the claimed method could allegedly be construed as being implemented without a computer (Office Action, page 4, paragraph 5.1).

Applicants do not acquiesce to this rejection. In order to expedite prosecution, however, Applicants amend claim 3 to recite "A computer-implemented method...". Therefore, Applicants submit that claim 3 complies with the requirements of 35 U.S.C. § 101. Moreover, Applicants respectfully request entry of the amendment since it does not require any further search and/or consideration.

Claim Rejections – 35 U.S.C. § 103

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,041,168 to Hasegawa ("Hasegawa '168") in view of U.S. Patent No. 5,528,511 to Hasegawa ("Hasegawa '511"). For *at least* the following reasons, Applicants respectfully traverse the rejection.

The Examiner's response to the previously submitted arguments is basically the same as the last Office Action dated July 9, 2008 (e.g., see current Office Action, page 18, last paragraph, and last Office Action, page 17, first full paragraph). The only difference in the current Office Action is lines 2-7 on page 19, but here, the Examiner again points to previously cited portions of the references which allegedly teach that manual judgment is not necessary in Hasegawa '511 for preparing the information indicated by the invalidness specifier of FIG. 7. Applicants respectfully disagree.

For example, in the Examiner's response on page 19 of the Office Action, it is alleged that Hasegawa '168, in col. 1, lines 58-61 and col. 2, lines 30-35 teaches a library that already contains logical operation information. Applicants submit, however, that this logical operation does not teach or suggest all the features of the claimed logical operation information. For example, the claimed logical operation information comprises delay time information which is

specific to an input terminal logical **state transition** and a resulting logical **state transition** at an output terminal. Although Hasegawa '168 discloses storing a delay time from each pin of a starting point in the logical circuit to a pin corresponding to the ending point, it does not teach or suggest that the stored delay time is specific to a state transition of the pin. Moreover, neither Hasegawa '511 nor Hasegawa '168 teach that the type of logic circuit which is the subject of delay analysis is prestored. As such, the delay analysis cannot be automatic, as required by claim 1. Consequently, Hasegawa '511 alone, or in combination with Hasegawa '168, does not render claim 1 obvious.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. Further, Applicants' respectfully remind the Examiner to contact the Applicants' representative at the telephone number listed below to resolve any points that remain at issue, per the Examiner's agreement during the aforementioned phone interview.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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